

AMENDMENTS TO THE DRAWINGS:

Please amend drawing figure sheet -1/5 to reflect addition of the "Prior Art" legend as provided in the Replacement Sheet attached hereto.

REMARKS

Reconsideration of the above-identified application, as amended, is respectfully requested.

In the Official Action dated June 1, 2005, the Examiner first objected to the drawings, particularly as not setting forth the Figure 1 series of figures as prior art. In response to the drawing objection, applicants submit a Replacement Marked-Up Drawing Sheet properly indicated with a "prior art" legend.

In the Official Action dated June 1, 2005, the Examiner further rejected to Claims 11-20 under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent Publication No. US 2003/0011080 to Deshpande et al. ("Deshpande").

With respect to the rejection of Claims 11-20, applicants respectfully disagree.

As a preliminary matter, Claim 2 is being canceled and the subject matter thereof being added to amended independent Claim 11. Thus, claim 11 sets forth a complementary metal oxide semiconductor (CMOS) structure comprising:

a gate region formed on a surface of a semiconductor substrate, said gate including an dielectric layer formed on exposed vertical sidewalls thereof and a substrate surface;

a vertical nitride spacer element formed on each vertical sidewall of the gate stack overlying said dielectric layer, whereby a portion of the dielectric layer underlies the vertical nitride spacer above the substrate surface such that an edge of the portion of the dielectric layer underlying the vertical nitride spacer is aligned with an outer edge of the vertical nitride spacer element; and,

a nitride plug formed over said gate stack, vertical nitride spacer elements and said edge of said portion of said dielectric layer underlying said vertical nitride spacer, said nitride plug encapsulating and sealing said underlying dielectric layer; and,

silicide contacts formed on other portions of said semiconductor substrate adjacent said patterned gate region, for contact with drain and source regions formed in said semiconductor substrate.

Furthermore, while Dishpande teaches a "L"-shaped dielectric spacer layer 23 (in Fig. 1D of Dishpande) between a patterned gate stack 14 and spacer element 24, the edge of the dielectric layer underlying the spacer is not aligned with the outer edge of the vertical nitride spacer element. In fact, quite the contrary, the L-shaped dielectric portion that underlies the spacer, has an edge that is purposefully recessed (See Figure 1D of Dishpande) forming a divot 26 (in Fig. 1D of Dishpande) underlying the spacer 24. In Dishpande, this divot is eventually filled by another material 28 (Fig. 1F of Dishpande) and requires several extra processing steps to accomplish.

With respect to the rejection of (now cancelled) Claim 12, while the Examiner has alleged that Dishpande in Figure 2D shows the vertical nitride spacer being aligned with the dielectric, applicants respectfully disagree. Dishpande, in Figure 2D does not teach a portion underlying the nitride spacer as being in edge-alignment with the outer edge of the vertical nitride spacer element as now claimed in amended Claim 1.

Moreover, Dishpande does not teach the provision of a nitride plug that is formed over the gate stack, vertical nitride spacer elements and the edge of the portion of the dielectric layer underlying the vertical nitride spacer.

In view of the foregoing, Applicants respectfully request the Examiner to withdraw rejection of amended independent Claim 11 and each its respective dependent claims under 35 USC §102(e).

In summary, it is respectfully submitted that this application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance be issued. If the Examiner believes that a telephone conference with the Applicants' attorneys would be advantageous to the disposition of this case, the Examiner is requested to telephone the undersigned.

Respectfully submitted,



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SF:gc
Attachment: One (1) Replacement Drawing Sheet